CLAIMS:

1. (Original) A data transferring apparatus for transferring liquid ejection data, comprising:

a decode circuit capable of performing hardware development on a liquid ejection data, which is DMA-transferred per word unit from a main memory via a system bus, compressed to be capable of line development; and

an invalid data mask processing means for nullifying data from head data, as many bytes as a remainder resulting from dividing a value of a data starting address of compressed liquid ejection data by the number of data bytes which said system bus can transfer per one data transfer, with respect to word data including head data of compressed data DMA-transferred from said main memory to said decode circuit.

2. (Cancelled)

3. (Currently Amended) A data transferring apparatus for transferring liquid ejection data as claimed in claim 1 [[or 2]], further comprising:

two independent buses which are said system bus and a local bus;

said main memory coupled to said system bus, capable of transferring data;

a local memory coupled to said local bus, capable of transferring data; and

a decode unit coupled to said system bus and local bus in order to transfer data therebetween, comprising:

a decode circuit;

a line buffer for storing liquid ejection data developed by said decode circuit per word unit; and

a DMA-transferring means for DMA-transferring liquid ejection data compressed to be capable of line development from said main memory to said decode circuit, DMA-transferring liquid ejection data developed in said line buffer to said local memory per word unit and DMA-transferring developed liquid ejection data stored in said local memory to a register of an liquid ejecting head sequentially.

4. (Original) A data transferring apparatus for transferring liquid ejection data as claimed in claim 3, wherein an ASIC comprises registers of said main memory, said decode unit and said liquid ejecting head as a circuit block respectively, and registers of said decode unit and said liquid ejecting head are coupled through an dedicated bus in said ASIC.

5. (Original) A data transferring apparatus for transferring liquid ejection data as claimed in claim 4, wherein said line buffer comprises two faces of buffer areas capable of storing developed data of predetermined words, liquid ejection data developed by said decode circuit is sequentially stored in a first face of said buffer areas while liquid ejection data developed by said decode circuit is sequentially stored in a second face of said buffer areas when developed data of predetermined words has been accumulated, and a developed data is DMA-transferred to said

local memory per predetermined words developed data of predetermined words has been accumulated.

6. (Original) A data transferring apparatus for transferring liquid ejection data as claimed in claim 5, wherein data transfers with respect to said local bus from said decode circuit to said local memory and from said local memory to a register of said liquid ejecting head are performed in a burst transfer.

7. (Original) A data transferring apparatus for transferring liquid ejection data as claimed in claim 6, wherein said compressed liquid ejection data is run length compressed data, and said decode circuit can perform hardware development on run length compressed data.

8. (Original) A data transferring apparatus for transferring liquid ejection data as claimed in claim 7, wherein said decode unit comprises a non-development processing means for storing uncompressed liquid ejection data DMA-transferred from said main memory in said line buffer without hardware development by said decode circuit.

9. (Original) A liquid ejecting apparatus comprising a data transferring apparatus for transferring liquid ejection data comprising:

a decode circuit capable of performing hardware development on liquid ejection data, which is DMA-transferred per word unit from a main memory via a system bus, compressed to be capable of line development; and

an invalid data mask processing means for nullifying data from head data, as many bytes as a remainder resulting from dividing a value of a data starting address of compressed liquid ejection data by the number of data bytes which said system bus can transfer per one data transfer, with respect to word data including head data of compressed data DMA-transferred from said main memory to said decode circuit.

Claims 10 – 50 (Cancelled).